ISSN 2348 – 9928
IJAICT Volume 3, Issue 12, December 2016 Doi:01.0401/ijaict.2014.07.14 Published on 05 (12) 2016

REVIEW ON FFT PROCESSOR FOR OFDM SYSTEM

Miss. Jaishri Katekhaye
PG Scholar,

Mr. Amit Lamba
Assistant Professor,

Mr. Vipin Bhure
Assistant Professor,

Electronics and Communication Engineering,
G. H. Raisoni Academy of Engineering and Technology,
Nagpur, Maharashtra, India

Abstract— ***Orthogonal frequency division multiplexing (OFDM) is a popular method for wireless transmission of data at high rate. To increase the speed of transmission, the input high rate data stream is divided into many small data streams which are then transmitted parallel in OFDM system. The key component of OFDM system is the FFT processor. FFT converts the input time domain signal into frequency domain at the receiver side. Efficient implementation of FFT processor with small area, low power and high speed is very important. This can be achieved with the help of various algorithms viz. radix-2, radix-4, radix-8. FFT processor with higher mixed radix (radix-8 and radix-2) algorithm is going to propose. As higher mixed radix algorithm reduces power and increases speed. This paper gives an overview of the work done on FFT processor previously.***

Keywords— FFT, Mixed Radix, OFDM, VHDL.

I. INTRODUCTION

Fast Fourier transform (FFT) are widely used in different areas of applications such as communications, radars, imaging, etc. One of the major concerns for researchers is to meet real-time processing requirements and to reduce hardware complexity mainly with respect to area and power and to improve processing speed.

Discrete fourier transform (DFT) is defined as

$$X[K] = \sum_{n=0}^{N-1} x[n].\ W_N^{nk} \qquad (1)$$

$$W_N^{nk} = e^{-j2\pi nk/N} \qquad 0 \le k \le N\text{-}1$$

Where X[k] and x[n] are frequency domain and time domain sequences. To compute all N values DFT requires N^2 complex multiplications and N(N-1) complex additions. Since the amount of computation and thus the computation time, is approximately proportional to N^2, it will cost a long computation time for large values of N. For this reason, it is very important to reduce the number of multiplications and additions. This algorithm is an efficient algorithm to compute the DFT, which is called Fast Fourier Transform (FFT) algorithm.

1.1 Radix-2

The radix-2 algorithms are the simplest FFT algorithms. The decimation-in-frequency (DIF) radix-2 FFT partitions the DFT computation into even-indexed and odd-indexed outputs, which can each be computed by shorter-length DFTs of different combinations of input samples.

$$X[K] = \sum_{n=0}^{N-1} x[n].\ W_N^{nk}$$

Radix-2 algorithm divides above equation into even and odd ordered samples.

$$X[K] = \sum_{n(even)} x(n) W_N^{kn} + \sum_{n(odd)} x(n) W_N^{kn} \qquad (2)$$

Following figure shows the basic block of the radix-2 butterfly unit which consists of two adders and one complex multiplier.

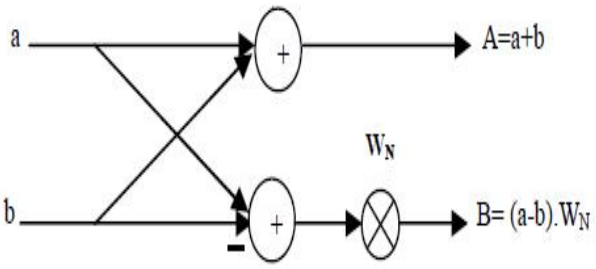

Fig 1 : Basic Butterfly Unit of Radix-2.

1.2 Radix-8

Radix-8 is another FFT algorithm which increases speed of functioning and this can be achieved by changing the base to 8 [2]. It operates on the DFT equation and divides it into eight N/8 point DFTs. The following equations illustrate radix-8 decimation in frequency (DIF).

ISSN 2348 – 9928
Doi:01.0401/ijaict.2014.07.14 Published on 05 (12) 2016

$$X[K] = \sum_{n=0}^{\frac{N}{8}-1} x(n)W_N^{kn} + \sum_{n=0}^{\frac{N}{8}-1} x\left(n+\frac{N}{8}\right)W_N^{k\left(n+\frac{N}{8}\right)} + \sum_{n=0}^{\frac{N}{8}-1} x\left(n+\frac{2N}{8}\right)W_N^{k(n+\frac{2N}{8})} + \sum_{n=0}^{\frac{N}{8}-1} x\left(n+\frac{3N}{8}\right)W_N^{k(n+\frac{3N}{8})} + \sum_{n=0}^{\frac{N}{8}-1} x\left(n+\frac{4N}{8}\right)W_N^{k(n+\frac{4N}{8})} + \sum_{n=0}^{\frac{N}{8}-1} x\left(n+\frac{5N}{8}\right)W_N^{k(n+\frac{5N}{8})} + \sum_{n=0}^{\frac{N}{8}-1} x\left(n+\frac{6N}{8}\right)W_N^{k(n+\frac{6N}{8})} + \sum_{n=0}^{\frac{N}{8}-1} x\left(n+\frac{7N}{8}\right)W_N^{k(n+\frac{7N}{8})} \quad (3)$$

The basic operation of radix-8 butterfly is shown in following figure.

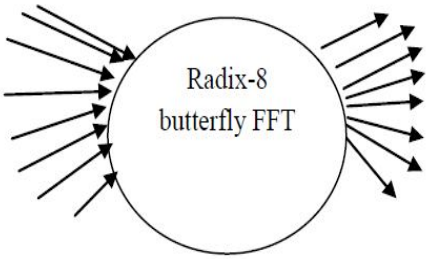

Fig 2 : Radix-8 Butterfly Unit.

1.3 Mixed-Radix

A mixed radix algorithm is an integration of different algorithms of radix number. Different radix algorithms are used in each step for computation of FFT. This algorithm gives a lot of choices in selecting the size of transformation. There are two types of mixed-radix FFT algorithms. In first category, in which a radix-*q* algorithm, where q=2*m* > 2, is applied to an input consisting of equally spaced points, where $1 \leq k < m$. In this, '*k*' steps of radix-2 algorithm are applied either at beginning or at the end of transformation. Another category indicates to those specialized for a composite $N=N0\times N1\times N2\ldots\times Nk$ [3].

1.4 FFT Architectures

Sequential Processor: The basic sequential processor comprises of a processing element (PE) which computes butterfly. The same memory can be used to store input, output data and intermediate results and twiddle factors. The amount of hardware required is very small and it takes sequential operations to compute the FFT.

Pipeline Processor: This architecture is also known as cascaded FFT architecture. For improving the performance of sequential processor, parallelism can be introduced by using separate arithmetic unit for each stage of the FFT processor which increases the throughput by a factor of when different units are pipelined.

Parallel Iterative Processor: Performance of FFT processor can be improved by adding more processing elements in each sequential pipeline stage. Butterflies are computed in parallel in each stage. Total execution time required is cycles for parallel iterative processor.

Array Analyzer: A fully parallel structure can be obtained which has processing element for each of the butterfly operations. This is not a good option for large N as it requires more hardware.

1.5 Block Diagram of FFT processor

The whole structure of FFT processor contains a butterfly processing unit, a RAM and ROM unit for the storage of data, a address generation unit and a sequential control unit. The important units of FFT processor are butterfly processing unit and address generation unit. The dual port RAM used to store input data and intermediate results and output. Twiddle factors are stored in ROM. The address generation unit generates the address for reading data for butterfly operations and also for storing the output results in RAM. Sequential control unit generates the control signals for each module.

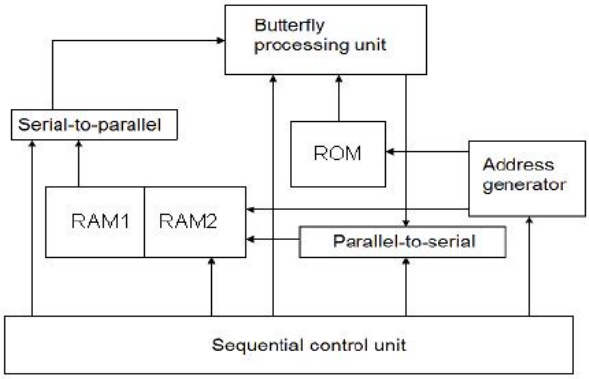

Fig 3: Block diagram of FFT processor

II. RELATED WORK DONE

"A Scalable FFT Processor Architecture for OFDM Based Communication Systems", in this paper radix-2 algorithm is used for FFT implementation. Also they proposed pipeline architecture. Pipeline architecture is also known as cascaded FFT architecture in which each stage has its own processing element. The proposed architecture operates at fixed and variable length FFT processor and gives good speed, flexibility and scalability. It supports any N-point FFT. Author proposed from 16-point to 2048-point. It meets the requirement of various wireless standards. ROM is used for the storage of twiddle factors. It is found that clock cycles required for 64-point FFT processor are 254. The time required for the computation of processor is 1.27μs. Also power required is 423.46mW [4].

ISSN 2348 – 9928
Doi:01.0401/ijaict.2014.07.14 Published on 05 (12) 2016

"VHDL Implementation of an Optimized 8-point FFT/IFFT processor in Pipeline Architecture for OFDM systems", in this paper a 8-point FFT processor is proposed using Radix-2 algorithm with R2MDC (Radix-2 multipath delay commutator) architecture. Here two methods are used to reduce the number of complex multiplications. In first method, the implemented algorithm for complex multiplication uses three multiplications, one addition and two subtraction and in second method add and shift operation is used for the reduction of complex multiplications. From the results it is observed that no. of complex multiplications required for first method=4 and for second method=0. Hence it achieves the target of less resource usage [5].

"VLSI Design of Mixed radix FFT Processor for MIMO OFDM in wireless Communications", in this paper author implemented 64-point FFT processor using mixed radix algorithm having combination of Radix-2 and Radix-4. Here bit reversal architecture is used for implementing FFT processor. It is done for multi input multi output (MIMO) OFDM system. Hence it meets the requirement of IEEE 802.11n WLAN standard. The proposed paper reduces the hardware complexity and hence power gets reduced as it is using mixed radix algorithm. It requires no. Of CLB slices=750 Utilization factor=9.77% and power=3831.63mW [6].

"Design of a Low Power 64 Point FFT Architecture for WLAN Applications", in this paper a 64-point FFT processor is implemented using radix-4^3 algorithm. Here three stages of radix-4 are used for the computation of FFT processor. A parallel unrolled radix-4^3 architecture is presented. This architecture accepts four inputs per clock cycle and produces four outputs per clock cycle. As compared to single path delay feedback (SDF) and multipath delay commutator (MDC), this architecture requires more hardware but reduces the clock rate to 25%. It operates at clock frequency of 100MHz. But to meet the time requirement of 3.2μs for IEEE 802.11a/g, the processor has to be operated at 5MHz with power dissipation of 2.27mW [7].

"Design and VLSI Implementation of A Radix-4 64- Point FFT Processor", in this paper author proposed a 64-point pipelined FFT processor using radix-4. It is implemented for WLAN applications. Twiddle factors are not stored in ROM instead twiddle factor generation unit is used. For the storage of input and output, dual port RAM is used. For the generation of control signals Micro Coded State Machine is implemented which generates all the control signals required for processor. The comparison is done on the basis of Radix-2 and Radix-4 algorithm. It is observed that delay required for implementing 64-point FFT using Radix-2=31.55ns and for Radix-4=29.688ns [8].

III. CONCLUSION

From the above related paper, we come to the conclusion that the radix-2 algorithm used in [4], [5] is very simple and requires more butterfly units as compared to the radix-4 used in [8]. The architecture presented in [7] greatly reduces the clock rate but hardware complexity increases. Twiddle factors are stored in ROM in [4] whereas twiddle factor generation unit is used in [8] which increase the hardware complexity. The FFT processor in [6] implemented using mixed-radix algorithm requires less number of CLB slices as compared to radix-2 and radix-4 and also there is less resource utilization. Hence we will propose higher mixed radix algorithm to design FFT processor.

References

[1] Sheng Zhou, Xiaochun Wang, Jianjun Ji, Yanqun Wang, "Design and Implementation of a 1024-point High-speed FFT Processor Based on the FPGA", 6th international congress on image and signal processing ©2013 IEEE.

[2] K.Sowjanya, Leele Kumari, "Design and Performance Analysis of 32 and 64 Point FFT using Radix-2 Algorithm",Proceedings of AECE-IRAJ International Conference, 14th July 2013.

[3] K. Umapathy, Dr. D. Rajaveerappa, "Implementation Of Optimized 128-Point Pipeline Fft Processor Using Mixed Radix 4-2 For OFDM Applications", International Journal of Engineering Science and Technology (IJEST) Vol. 4 No.12 December 2012.

[4] Deepak Revanna, Omer Anjum, Manuele Cucchi, Roberto Airoldi, Jari Nurmi, "A Scalable FFT Processor Architecture for OFDM Based Communication Systems".978-1-4799-0103-6/13/$31.00 ©2013 IEEE.

[5] Mounir Arioua, Said Belkouch, Mohamed Agdad, Moha M'rabet Hassani, "VHDL Implementation of an Optimized 8-point FFT/IFFT processor in Pipeline Architecture for OFDM systems", 978-1-61284-732-0/11/$26.00 ©2010IEEE.

[6] N Kirubanandasarathy , Dr.K.Karthikeyan & K.T hirunadanasikamani, "VLSI Design of Mixed radix FFT Processor for MIMO OFDM in wireless Communications", 978-1-4244-7770-8/10/$26.00 ©201 0 IEEE.

[7] Kala S, Nalesh S, S K Nandy, Ranjani Narayan, "Design of a Low Power 64 Point FFT Architecture for WLAN Applications", 978-1-4799-3570-3/13/$31.00 ©2013 IEEE.

[8] M.Vijaya kumar, M.Vidya and G.Sriramulu, "Design and VLSI Implementation of A Radix-4 64 - Point FFT Processor". International Journal of Research in Computer and Communication technology, IJRCCT, ISSN 2278-5841, Vol 1, Issue 7, December 2012.